REMARKS

Reconsideration of this application as amended is respectfully requested. Claims 1, 17 and 23 have been amended. The claim amendments are fully supported by the specification or drawing. No new matter has been added. Applicant's remarks below are directed to the claims as amended herein.

Claim Rejections – 35 U.S.C. § 102(a)

Claims 1-27 have been rejected under 35 U.S.C § 102(a) as being anticipated by U.S. Patent Publication 2002/0083255 of Greeff et al. ("Greeff"). Applicant respectfully submits that claims 1-27 are not anticipated by Greeff.

Claim 1 recites, in part:

> an interface device coupled to the memory controller via a first signal path that is permanently terminated at the interface device

Greeff discloses interface circuits for connecting memory modules to a segmented data bus (Greeff, paragraph 0031), with each interface circuit including a switching circuit to optionally connect a given bus segment with a downstream bus segment for optional pass-through of data on the segmented bus (Greeff, paragraph 0041). That is, the switching circuit is configured to disconnect the bus segment from the downstream bus segment while the interface circuit is receiving transmitted data and to connect the bus segment to the downstream bus segment while the interface circuit is not selected for operations (Greeff, para. 0042). Thus, Greeff does not disclose or suggest a first signal path that is permanently terminated at an interface device as recited in applicant's claim 1, but rather a bus segment that is selectively connected to or disconnected from a downstream bus segment according to whether the corresponding interface circuit is selected to receive transmitted data. In view of this clear distinction, applicant submits that claim 1 is not anticipated or rendered obvious by Greeff.

Because claims 2-16 depend from and further limit claim 1, applicant submits that claims 2-16 also are not anticipated or rendered obvious by Greeff.

Claim 17 recites, in part:

> transmitting multiplexed data from a memory controller to an interface device at a first data rate via a signal path that is

permanently terminated at the interface device

Applicant submits that, at least for the reasons given above in reference to claim 1, Greeff does not disclose or suggest the above-recited limitation, and therefore that claim 17 is not anticipated or rendered obvious by Greeff. Because claims 18-22 depend from and further limit claim 17, applicant submits that claims 18-22 also are not anticipated or rendered obvious by Greeff.

Claim 23 recites, in part:

> a first input/output (I/O) port to receive multiplexed data from a memory controller at a first signaling rate via a signal path that is permanently terminated at the interface device

Applicant submits that, at least for the reasons given above in reference to claim 1, Greeff does not disclose or suggest the above-recited limitation, and therefore that claim 23 is not anticipated or rendered obvious by Greeff. Because claims 24-27 depend from and further limit claim 23, applicant submits that claims 24-27 also are not anticipated or rendered obvious by Greeff.

Conclusion

Applicant respectfully submits that claims 1-27 are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

A Petition for Extension of Time is enclosed herewith.

Authorization is hereby given to charge deposit account 501914 for any fee deficiency associated with this Amendment.

Respectfully submitted,

SHEMWELL GREGORY & COURTNEY LLP

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